REMARKS

This response and amendment is submitted in response to the non-final Office Action dated February 3, 2005 (hereafter "office action"), having a shortened three-month statutory period set to expire May 3, 2005. The examiner had rejected pending claims 1 to 6, 10 to 16 and 20 for various reasons stated in the office action. The examiner found allowable subject matter in claims 7 to 9 and 17 to 19, and applicants appreciate the examiner's allowance of these claims in the office action.

I. Rejections under 35 U.S.C. Secs. 102

The examiner rejected claims 1 to 6, 10 to 16, and 20 under 35 U.S.C. Sec. 102(e) as being anticipated by U.S. Patent No. 6,476,671 to Tang (hereafter "the Tang reference") for various reasons indicated in the office action. However, applicants have amended the broad independent claims 1 and 11 to now explicitly recite that each of the at least two chopping amplifier stages contributes a partial gain amount to an overall gain of the chopping amplifier and the overall gain is a sum of the partial gain amounts of the at least two chopping amplifier stages. The Tang reference does not in any way teach or suggest such contributions of partial gain amounts of chopping amplifier stages to an overall gain of a chopping amplifier. The Tang reference also does not in any way teach or suggest that the overall gain is provided by the sum of the partial gain amounts.

The Tang reference instead teaches that only one of the amplifiers performs the traditional chopping operation and provides the entire gain at a time for the overall

system. In other words, the amplifiers in the Tang reference alternate among each other as to which one chops and provides the entire gain for the overall system, and the amplifiers do not in any way just each contribute a partial gain amount for the overall system gain. For example, the Tang reference discloses in the summary of the invention at column 2, lines 4 to 10 the following:

> The novel ping-pong amplifier includes respective nulling amplifiers for each of its gain amplifiers, which auto-zero each gain amplifier. In addition, switches are included which allow the differential inputs and outputs of the gain amplifiers to be chopped. Thus, while one gain amplifier is being auto-zeroed, the other gain amplifier amplifies the input signal while its inputs and outputs are chopped.

Thus, claims 1 and 11, as amended, are not anticipated by the Tang reference and are therefore allowable. Also, dependent claims 2 to 10 and 12 to 20 are at least allowable for the same reasons that respective claims 1 and 11 are allowable.

Furthermore, contrary to the examiner's assertion that all of the elements are disclosed in the Tang reference with respect to claims 5 and 15 in the office action, the elements of staggering chop clock signals of at least two chopping amplifier stages so that the chop clock signals of the at least two chopping amplifier stages have non-overlapping periods and at least one of the at least two chopping amplifier stages is not operating in an open loop at any given time, is not, so the rejection is unsupported by the art and should be withdrawn. Thus, claims 5 and 15 are allowable for this further reason.

Claims 6 and 16 have been amended to further recite that low-level aliasing due to chopping is also avoided. Additionally, contrary to the examiner's assertion that all of

the elements are disclosed in the Tang reference with respect to claims 6 and 16 in the office action, the elements of the non-overlapping periods are periodic non-overlapping periods so that a master chop clock of the master controller can be operated at a lower chop clock frequency and low-level aliasing due to chopping is avoided, is not, so the rejection is unsupported by the art and should be withdrawn. Thus, claims 6 and 16 are allowable for this further reason.

New claims 21 and 23 have been added as dependent from respective claims 17 and 7 and are allowable for at least the same reasons as claims 17 and 7. Also, with respect to claims 21 and 23, the Tang reference does not in any teach or suggest the non-overlapping periods are periodic non-overlapping periods so that a master chop clock of the master controller can be operated at a lower chop clock frequency fc and low-level aliasing due to chopping is avoided wherein the lower chop clock frequency fc is set equal to a sampling frequency fs / (2 * N). Thus, claims 21 and 23 are allowable for this further reason.

New claims 22 and 24 have been added as dependent from respective claims 11 and 1 and are allowable for at least the same reasons as claims 22 and 24. Additionally, with respect to claims 22 and 24, the Tang reference does not in any way teach or suggest that during non-switch transition periods, all of the at least two chopping amplifier stages are active and chopping, and during a switch transition period, one of the at least two chopping amplifier stages is disconnected while all remaining ones of the at least two chopping amplifier stages are chopping. Thus,

claims 22 and 24 are allowable for this further reason.

The specification, drawings, and claims as originally filed fully support the respective amendments or additions to the claims. Therefore, the application with pending claims 1 to 24, as respectively amended or added, is now in condition for allowance, and allowance is earnestly solicited. Applicants respectfully request that a timely Notice of Allowance be issued in this case.

No fees other than for additional claims are believed to be due by the filing of this Response and Amendment; however, if any other fees are due by the filing of the enclosed documents, including any fees incurred by an extension of term, please consider this paragraph such a Request for term, and charge any fees associated with the Request or any other fees incurred by the filing of this document to Cirrus Logic Deposit Account No. 03-2028/1410-CA.

Respectfully submitted,

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